AMENDMENTS TO THE CLAIMS

1. (Currently amended) A ferroelectric integrated circuit memory comprising:

a three-dimensional ("3-D") capacitor laminate, said capacitor laminate comprising a bottom electrode, a ferroelectric film, and a top electrode;

wherein said 3-D capacitor laminate comprises a 3-D shape having substantial directional components in three mutually orthogonal planes, ~~and~~ said ferroelectric film has a thickness not exceeding 80 nm, and said capacitor laminate has a thickness not exceeding 200 nm.

Claim 2 (Canceled)

3. (Original) A ferroelectric integrated circuit memory as in claim 1 wherein said ferroelectric film has a thickness not exceeding 60 nm.

4. (Original) A ferroelectric integrated circuit memory as in claim 1 wherein said ferroelectric film comprises ferroelecuric layered superlattice material.

5. (Original) A ferroelectric integrated circuit memory as in claim 4 wherein said ferroelectric film comprises strontium bismuth tantalate.

Claims 6 and 7 (Canceled)

8. (Original) A ferroelectric integrated circuit memory as in claim 1 wherein said laminate defines a capacitance area and a capacitor-footprint area, and said capacitance area exceeds said capacitor-footprint area.

9. (Original) A ferroelectric integrated circuit memory as in claim 8 wherein said capacitance area is at least two times greater than said capacitor-footprint area.

10. (Original) A ferroelectric integrated circuit memory as in claim 8 wherein said capacitance area is at least three times greater than said capacitor-footprint area.

11. (Original) A ferroelectric integrated circuit memory as in claim 8 wherein said capacitance area is at least four times greater than said capacitor-footprint area.

12. (Original) A ferroelectric integrated circuit memory as in claim 8 wherein said capacitor-footprint area does not exceed 0.5 nm^2.

13. (Original) A ferroelectric integrated circuit memory as in claim 8 wherein said capacitor-footprint area does not exceed 0.2 nm^2.

14. (Original) A ferroelectric integrated circuit memory as in claim 1, comprising a plurality of capacitor laminates.

15. (Original) A ferroelectric integrated circuit memory as in claim 1 wherein said bottom electrode, said ferroelectric film, and said top electrode conform substantially to said 3-D shape.

16. (Original) A ferroelectric integrated circuit memory as in claim 1, further comprising a nonconductive hydrogen barrier layer disposed above said capacitor laminate, said nonconductive hydrogen barrier layer comprising strontium tantalate.

17. (Original) A ferroelectric integrated circuit memory as in claim 1, further including a trench formed in a portion of said integrated circuit, and wherein said 3-D capacitor laminate is formed in said trench.

18. (Original) A ferroelectric integrated circuit memory as in claim 17, further comprising:

an insulator layer having an insulator top surface, and

wherein said trench is located substantially in said insulator layer, said trench having a trench bottom, a trench sidewall, and a trench opening substantially coplanar with said insulator top surface;

said bottom electrode substantially conforms to said trench bottom and said trench sidewall;

said ferroelectric film is disposed above said bottom electrode layer and substantially conforms to said bottom electrode; and

said top electrode is disposed above said ferroelectric film and substantially conforms to said ferroelectric film.

19. (Original) A ferroelectric integrated circuit memory as in claim 17 wherein said ferroelectric film has a thickness not exceeding 60 nm.

20. (Original) A ferroelectric integrated circuit memory as in claim 17 wherein said ferroelectric film comprises ferroelectric layered superlattice material.

21. (Original) A ferroelectric integrated circuit memory as in claim 17 wherein said bottom electrode, said ferroelectric film, and said top electrode define a capacitance area and a capacitor-footprint area, and said capacitance area is at least two times greater than said capacitor-footprint area.

22. (Original) A ferroelectric integrated circuit memory as in claim 21 wherein said capacitance area is at least three times greater than said capacitor-footprint area.

23. (Original) A ferroelectric integrated circuit memory as in claim 22 wherein said capacitance area is at least four times greater than said capacitor-footprint area.

24. (Original) A ferroelectric integrated circuit memory as in claim 21 wherein said capacitor-footprint area does not exceed 0.5 nm^2.

25. (Original) A ferroelectric integrated circuit memory as in claim 24 wherein said capacitor-footprint area does not exceed 0.2 nm^2.

26. (Original) A ferroelectric integrated circuit memory as in claim 18 wherein:
said 3-D capacitor laminate has a laminate thickness and a top laminate surface; and
wherein said insulator top surface and said trench bottom define a trench depth; and
wherein said laminate thickness is less than said trench depth.

27. (Original) A ferroelectric integrated circuit memory as in claim 26 wherein said laminate thickness does not exceed 300 nm.

28. (Original) A ferroelectric integrated circuit memory as in claim 26 wherein said laminate thickness does not exceed 200 nm.

29. (Original) A ferroelectric integrated circuit memory as in claim 26 wherein said trench opening has a trench opening area and said top laminate surface has a laminate area, said laminate area being greater than said trench opening area.

30. (Original) A ferroelectric integrated circuit memory as in claim 29 wherein laminate area is more than two times greater than said trench opening area.

31. (Original) A ferroelectric integrated circuit memory as in claim 29 wherein said trench opening area does not exceed 0.5 nm^2.

32. (Original) A ferroelectric integrated circuit memory as in claim 29 wherein said trench opening area does not exceed 0.2 nm^2.

33. (Original) A ferroelectric integrated circuit memory as in claim 17, comprising a plurality of trenches and a plurality of corresponding capacitor laminates.

34. (Original) A ferroelectric integrated circuit memory as in claim 33 wherein a distance between two adjacent trenches does not exceed 250 nm.

35. (Original) A ferroelectric integrated circuit memory as in claim 17, further comprising a nonconductive hydrogen barrier layer disposed above said capacitor laminate, said nonconductive hydrogen barrier layer comprising strontium tantalate.

36. (Original) A ferroelectric integrated circuit memory as in claim 1, further including a pillar formed in a portion of said integrated circuit, and wherein said 3-D capacitor laminate is formed on said pillar.

37. (Original) A ferroelectric integrated circuit memory as in claim 36 wherein:

said pillar is formed of insulating material, said pillar having a pillar top surface and a pillar sidewall;

said bottom electrode covers a portion of said pillar, said bottom electrode substantially conforming to said pillar top surface and to a portion of said pillar sidewall;

said ferroelectric film is disposed above said bottom electrode layer, said ferroelectric film substantially conforming to said bottom electrode; and

said top electrode is disposed above said ferroelectric film, said top electrode substantially conforming to said ferroelectric film.

38. (Currently amended) A ferroelectric integrated circuit memory as in claim 37 wherein said ferroelectric film has a thickness [[is]] not exceeding 60 nm.

39. (Original) A ferroelectric integrated circuit memory as in claim 38 wherein said ferroelectric film comprises ferroelectric layered superlattice material.

40. (Original) A ferroelectric integrated circuit memory as in claim 38 wherein said bottom electrode, said ferroelectric film, and said top electrode define a capacitance area and a capacitor-footprint area, and said capacitance area exceeds said capacitor-footprint area.

41. (Original) A ferroelectric integrated circuit memory as in claim 40 wherein said capacitance area is at least two times greater than said capacitor-footprint area.

42. (Original) A ferroelectric integrated circuit memory as in claim 40 wherein said capacitance area is at least three times greater than said capacitor-footprint area.

43. (Original) A ferroelectric integrated circuit memory as in claim 40 wherein said capacitance area is at least four times greater than said capacitor-footprint area.

44. (Original) A ferroelectric integrated circuit memory as in claim 40 wherein said capacitor-footprint area does not exceed 0.5 nm^2.

45. (Original) A ferroelectric integrated circuit memory as in claim 40 wherein said capacitor-footprint area does not exceed 0.2 nm^2.

46. (Original) A ferroelectric integrated circuit memory as in claim 36 wherein:
said 3-D capacitor laminate has a laminate thickness and a top laminate surface; and
wherein said pillar sidewall defines a pillar height; and
wherein said laminate thickness is less than said pillar height.

Claims 47 and 48 (Canceled)

49. (Original) A ferroelectric integrated circuit memory as in claim 46 wherein said pillar top surface has a pillar top area and said top laminate surface has a laminate area, said laminate area being greater than said pillar top area.

50. (Original) A ferroelectric integrated circuit memory as in claim 49 wherein laminate area is more than two times greater than said pillar top area.

51. (Original) A ferroelectric integrated circuit memory as in claim 49 wherein said pillar top area does not exceed 0.5 nm^2.

52. (Original) A ferroelectric integrated circuit memory as in claim 49 wherein said pillar top area does not exceed 0.2 nm^2.

53. (Original) A ferroelectric integrated circuit memory as in claim 36, comprising a plurality of pillars and a plurality of corresponding capacitor laminates.

54. (Original) A ferroelectric integrated circuit memory as in claim 53 wherein a distance between two adjacent pillars does not exceed 250 nm.

55. (Original) A ferroelectric integrated circuit memory as in claim 36, further comprising a nonconductive hydrogen barrier layer disposed above said capacitor laminate, said nonconductive hydrogen barrier layer comprising strontium tantalate.

Claims 56 – 71 (Canceled)

72. (Currently amended) A ferroelectric integrated circuit memory comprising:

a transistor;

an interlayer dielectric overlying said transistor;

a three-dimensional ("3-D") capacitor laminate, said capacitor laminate comprising a bottom electrode, a ferroelectric film, and a top electrode;

wherein said 3-D capacitor laminate comprises a 3-D shape having substantial directional components in three mutually orthogonal planes; and

wherein said capacitor laminate is formed on a conducting plug passing through said interlayer dielectric and having a height that is greater than the height of said transistor ~~has a thickness not exceeding 250 nm.~~

73. (Original) A ferroelectric integrated circuit memory as in claim 72 wherein said capacitor laminate has a thickness not exceeding 200 nm.

74. (Original) A ferroelectric integrated circuit memory as in claim 72 wherein said laminate defines a capacitance area and a capacitor-footprint area, and said capacitance area exceeds said capacitor-footprint area.

75. (Original) A ferroelectric integrated circuit memory as in claim 74 wherein said capacitance area is at least two times greater than said capacitor-footprint area.

76. (Original) A ferroelectric integrated circuit memory as in claim 74 wherein said capacitance area is at least three times greater than said capacitor-footprint area.

77. (Original) A ferroelectric integrated circuit memory as in claim 74 wherein said capacitance area is at least four times greater than said capacitor-footprint area.

78. (Original) A ferroelectric integrated circuit memory as in claim 74 wherein said capacitor-footprint area does not exceed 0.5 nm^2.

79. (Original) A ferroelectric integrated circuit memory as in claim 74 wherein said capacitor-footprint area does not exceed 0.2 nm^2.

80. (Original) A ferroelectric integrated circuit memory as in claim 72 wherein said ferroelectric film has a thickness not exceeding 80 nm.

81. (Original) A ferroelectric integrated circuit memory as in claim 72 wherein said ferroelectric film has a thickness not exceeding 60 nm.

82. (Previously presented) A ferroelectric integrated circuit memory comprising:

a three-dimensional ("3-D") capacitor laminate, said capacitor laminate comprising a bottom electrode, a ferroelectric film, and a top electrode;

wherein said 3-D capacitor laminate comprises a 3-D shape having substantial directional components in three mutually orthogonal planes;

wherein said ferroelectric integrated circuit memory further comprises a nonconductive hydrogen barrier layer disposed above said capacitor laminate, said nonconductive hydrogen barrier layer comprising strontium tantalate.